REMARKS

Claims 1-25 are all the claims pending in the application. Claims 1-3 and 7-22 are rejected. Claims 4-6 and 23-25 are allowed. Claim 1 is amended in order to secure the allowance of all of the claims. Claim 7 is cancelled.

The amendment to claim 1 is based on the content of claim 7.

Claim Rejections - 35 USC § 102

Claims 1, 7-10, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by WIPO document WO 99/13692 to Cambridge Display Technology Limited (herein referred to as "Cambridge"). This rejection is traversed for at least the following reasons.

First, with regard to claim 7, the rejection is moot in view of the cancellation of the claim.

Law of Anticipation

Second, basic U.S. Patent Law provides with respect to rejections under Section 102 that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In other words, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (MPEP §2131).

Amended Claim 1

Third, claim 1, which is directed to a method of making a transistor having plural layers, including a semiconductive layer and a dielectric layer, includes a step of "depositing on the first electrode a layer of a solution, said solution comprising material for forming the semiconductive layer and material for forming the dielectric layer. The claim now has been amended to further provide that the solution "comprises a diblock polymer, said diblock polymer comprising a semiconductive block for forming the semiconductive layer and a dielectric block for forming the dielectric layer."

This feature, which is taken from claim 7, is not found in Cambridge, nor would it be obvious from the teachings of the reference.

Cambridge

In framing the rejection based on Cambridge, the Examiner has made specific reference to page 2, last paragraph; page 5, line 25 to page 6, line 6; page 9, lines 7-27; and page 20, lines 3-25. Applicants respectfully submit that none of the cited text is relevant to the present invention.

No Relevant Teaching in Cited Sections of Cambridge

Applicants' understanding of the cited sections is that they describe a technique that involves alternately immersing a substrate in solutions of oppositely charged polymer materials to form respective sub-layers. Applicants submit that there is no reference in the cited sections of WO 99/13692 to immersing the substrate in a solution comprising both a material for forming a semiconductive layer and a material for forming a dielectric layer. Indeed, there is no disclosure of the specific limitation added to claim 1. Thus, there can be no anticipation.

The Examiner appears to be of the view that the stack ("self-assembled polymer layer") of alternating oppositely charged sub-layers mentioned at the cited sections of WO 99/13692 is a stack of sub-layers comprising both insulating sub-layers and semiconducting sub-layers in a single stack. However, Applicants respectfully submit that the teaching at page 5 of WO 99/13692 is that of forming a stack ("self-assembled polymer layer") of sub-layers, where the sub-layers in the stack are either all insulating layers, or all semiconductive layers, or all conductive layers. There is no teaching of two different layers, namely a semiconductor layer and a dielectric layer, both formed from the same solution.

No Disclosure of Single Solution With Two Different Units

With regard to cancelled claim 7, which is the basis for the present amendment to claim 1, the Examiner has made specific reference to Figures 2(a) to 2(d) of WO 99/13692. In particular, the Examiner has made reference to the insulating polymer materials illustrated at Figures 2(a) and 2(b) and to the semiconductive polymer materials illustrated at Figures 2(c) and 2(d) of WO 99/13692.

However, Applicants respectfully submit that at pages 5 and 6 of WO 99/13692 there is no disclosure of using a polymer comprising a combination of one or more units according to Figures 2(a) and/or 2(b) and one or more of units according to Figures 2(c) and/or 2(d). In

particular, there is no disclosure of providing a polymer comprising a block of successive units according to Figure 2(a) and/or 2(b) and a block of successive units according to Figure 2(c) and/or 2(d).

Page 5, lines 25 to 28 of WO 99/13692 refers to an insulating polymer (for one sub-layer) formed from a solution comprising the structure of Figure 2(a), and an insulating polymer (for another sub-layer) formed from a solution comprising the structure of Figure 2(b).

Page 5, line 29 to page 6 , line 1 of WO 99/13692 refers to a semiconducting polymer (for one sub-layer) formed from a solution comprising the structure of Figure 2(c), and a semiconducting polymer (for another sub-layer) formed from a solution comprising the structure of Figure 2(d).

No Disclosure of Diblock Polymer

Applicants respectfully submit that there is no disclosure of any polymer comprising a combination of the unit types illustrated in Figures 2(a) to 2(d), and particularly no disclosure of diblock polymer comprising a sequence of one of the unit types and a sequence of a different one of the unit types.

A diblock polymer can be represented by the formula An-Bm, where An is a series of n units of type A and Bm is a series of m units of type B. Applicants submit that the Examiner cannot find any disclosure of a diblock polymer at the cited sections of WO 99/13692. As mentioned above, the polymers described at page 5, line 12 to page 6, line 1 of WO 99/13692 with reference to Figures 2(a) to 2(d) comprise only one unit type, i.e. a unit type according to one of Figures 2(a) to 2(d), and are not block polymers.

No Anticipation

On the basis of applicable law and the deficiencies in the teachings of Cambridge, there can be no anticipation. The rejection should be withdrawn.

Claim Rejections - 35 USC § 103

Claims 2, 3, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over WIPO document WO 99/13692, issued by Cambridge Display Technology Limited (herein referred to as "Cambridge"). This rejection is traversed for at least the following reasons.

Claims 2 and 3 would be patentable because of their dependence on amended claim 1, for the reasons already given.

Moreover, the Examiner admits with regard to claim 2 that Cambridge fails to teach the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) is in the range of from 0.5 to 2.

The Examiner asserts that, "given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See In re Aller, Lacey, and Hall (10 USPQ 23 3-237) " However, given the significant differences in structure, as noted for amended claim 1, the features of claims 2 and 3 would not be obvious as the basic solution and diblock structure is not shown in Cambridge.

With regard to claim 13, which depends from claim 11, the Examiner admits that Cambridge fails to teach the material for forming the dielectric layer has a surface tension in the range of from 15 to 35 dyn/cm. However, claim 11 has not been rejected on the basis of Cambridge alone. Indeed, the Examiner admits that claim 11 is not met by Cambridge alone, having to rely on Marks in framing the rejection next recited. Moreover, claim 11 depends from claim 1, which has been demonstrated as being patentable over Cambridge alone. Thus, for several reasons, the rejection of claim 13 cannot be sustained

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Marks et al, US Patent 5,834,100. This rejection is traversed for at least the following reasons.

Claim 11 depends from claim 1. The Examiner admits that Cambridge fails to teach that the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density. The Examiner looks to Marks for a teaching that "the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density (abstract) by teaching the use of siloxane as an appropriate material for an OLED device to provide an environmentally stable material over prolonged use of the device over a period of time." However, Marks is not cited to remedy the deficiencies of Cambridge with regard to the use of a diblock polymer in a solution, one of the polymers being a semiconductor block and the other

being a dielectric block that form respective layers. Thus, claim 11 would be patentable over the combination of references.

Claim 12, which depends from claim 11, would be patentable because of that dependency.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Cheng et al, US Patent 6,737,303. This rejection is traversed for at least the following reasons.

Regarding claim 14, which depends from amended claim 1, the Examiner admits that Cambridge fails to teach the transistor is in top-gate configuration. The Examiner looks to Cheng solely for a teaching of a transistor that "is in top-gate configuration (figure 3) which is another alternative type of semiconductor device with a polymer layer that may be formed using a self-assembling process to form said polymer layer for a top-gate transistor."

As Cheng does not remedy the deficiencies of Cambridge, as detailed with regard to parent amended claim 1, the rejection is overcome.

Claims 15-17, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Dimitrakopoulos et al, US Patent 5,981,970. This rejection is traversed for at least the following reasons.

Regarding claim 15, which depends from amended claim 1, the Examiner admits that Cambridge fails to teach the transistor is in bottom-gate configuration. The Examiner looks to Dimitrakopoulos for a teaching of a transistor that "is in bottom-gate configuration (figure 6) as an alternative type of semiconductor device which also uses a self-assembling layer to form a polymer material for a bottom-gate semiconductor device."

As Dimitrakopoulos does not remedy the deficiencies of Cambridge, as detailed with regard to parent amended claim 1, the rejection is overcome.

Regarding claims 16 and 17, which depend from claim 15, the claims would be patentable because of that dependency.

Regarding claim 20, which depends from amended claim 1, the Examiner admits that Cambridge fails to teach the transistor is a field-effect transistor. The Examiner looks to

Dimitrakopoulos for a teaching of a transistor that is "a field-effect transistor (figure 6) as an alternative type of semiconductor device which also uses a self-assembling layer to form a polymer material for a bottom-gate semiconductor device."

As Dimitrakopoulos does not remedy the deficiencies of Cambridge, as detailed with regard to parent amended claim 1, the rejection is overcome.

Regarding claim 22, which depends from amended claim 1, the Examiner admits that Cambridge fails to teach the transistor is obtainable by the method as defined in claim 1. The Examiner looks to Dimitrakopoulos for a teaching of a transistor that is "obtainable by the method as defined in claim 1 (figure 6) as an alternative type of semiconductor device which also uses a self assembling layer to form a polymer material for a bottom-gate semiconductor device."

As Dimitrakopoulos does not remedy the deficiencies of Cambridge, as detailed with regard to parent amended claim 1, the rejection is overcome.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cambridge as applied to claims above, and further in view of Narayan (US Patent Application 2002/0084504). This rejection is traversed for at least the following reasons.

Claim 21 depends from amended claim 1. The Examiner admits that Cambridge fails to teach the transistor is a phototransistor. The Examiner looks to Narayan for a teaching that "the transistor is a phototransistor (figure 1 B), which is another alternative type of semiconductor device with a polymer layer that may be formed using a self-assembling process to form said polymer layer." However, Narayan is not cited to remedy the deficiencies of Cambridge with regard to the use of a diblock polymer in a solution, one of the polymers being a semiconductor block and the other being a dielectric block that form respective layers. Thus, the rejection is overcome.

Allowable Subject Matter

Claims 4-6 and 23-25 are allowed. In the statement of reasons for the indication of allowable subject matter, the Examiner notes that claim 4 requires a semiconductive layer comprising a **semiconductive polymer** and a dielectric layer comprising an **insulating polymer,**

wherein the method comprises the steps of (i) depositing on the first electrode a layer of a solution, said solution comprising material for forming the semiconductive layer and material for forming the dielectric layer, wherein the material for forming the dielectric layer is mixed with the material for forming the semiconductive layer in the solution. Applicants respectfully submit that the same reasoning would support patentability for amended claim 1 and the claims dependent therefrom,, as articulated above.

Thus for the foregoing reasons, all of claims 1-6 and 8-31 should be allowed.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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23373
CUSTOMER NUMBER

Date: September 10, 2009